SH6620A

Mask 4-bit Microcontroller

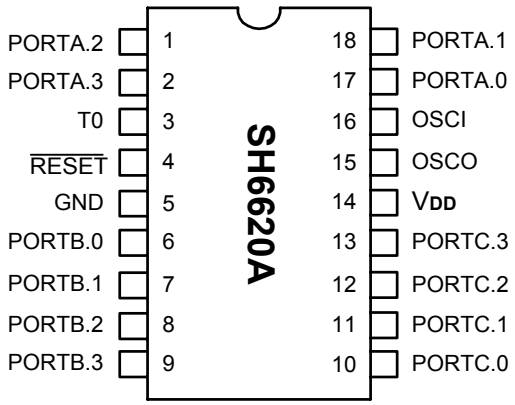
Features

- SH6610C-based single-chip 4-bit micro-controller.
- ROM: 1K X 16 bits.
- RAM: 64 X 4 bits (Data memory).
- Operation voltage: 2.2V - 6.0V (Typical 3.0V or 5.0V).
- 12 CMOS bi-directional I/O pins.
- 4-level subroutine nesting (including interrupts).
- One 8-bit auto re-loadable timer/counter.
- Warm-up timer for power-on reset.
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - External interrupts: PortB & PortC (Falling edge).
- Oscillator (code option)
  - X`tal oscillator: 32.768KHz ~ 4MHz.
  - Ceramic resonator: 400K ~ 4MHz.
  - RC oscillator : 400K ~ 4MHz.
  - External clock: 30K ~ 4MHz.
- Instruction cycle time:
  - 4/32.768KHz (≈ 122us) for 32.768KHz OSC clock.
  - 4/4MHz (= 1us) for 4MHz OSC clock.
- Two low power operation modes: HALT and STOP.
- Built-in watchdog timer (code option)

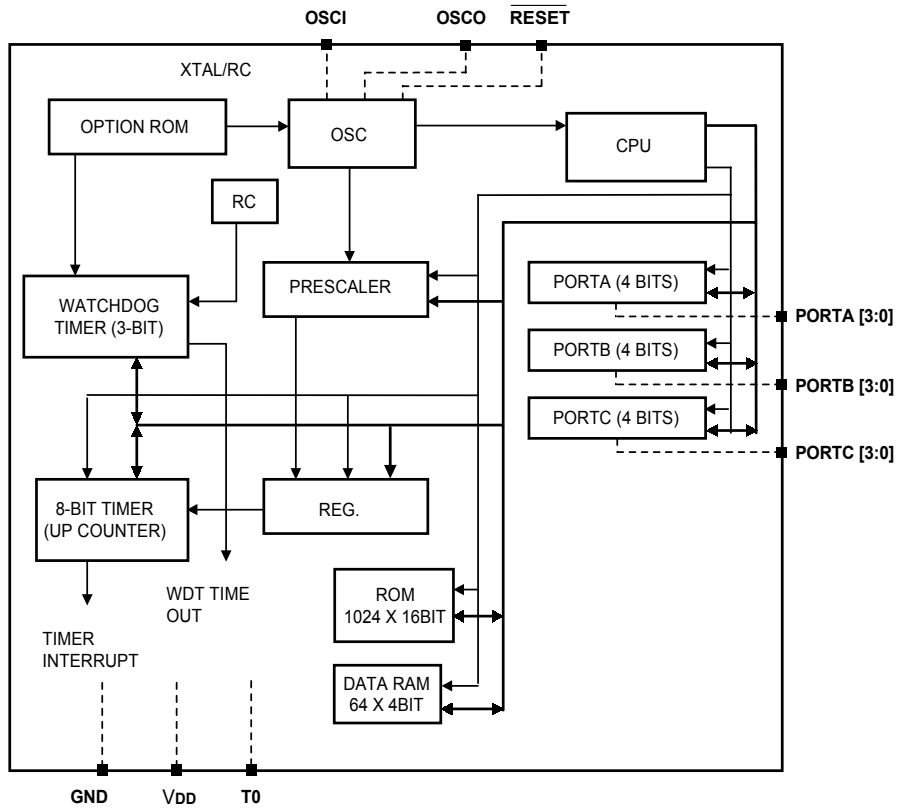
General Description

SH6620A is a 4-bit microcontroller. This chip integrates the SH6610C 4-bit CPU core with SRAM, 1K program of ROM, Timer and I/O Ports.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Designation	I/O	Description
1 - 2	PORTA2, 3	I/O	Bit programmable I/O pins
3	T0	I	Timer Clock/Counter (Schmitt Trigger input)
4	$\overline{\text{RESET}}$	I	Reset input (Active Low) (Schmitt Trigger input)
5	GND	P	Ground
6 - 9	PORTB0 - 3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge)
10 - 13	PORTC0 - 3	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge)
14	V_{DD}	P	Power Supply
15	OSCO	O	OSC output pin. There is a signal with a frequency of $F_{osc}/4$ for RC mode
16	OSCI	I	OSC input pin can be connected to crystal、 ceramic or external resistor
17 - 18	PORTA0, 1	I/O	Bit programmable I/O pins

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 1K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjust for addition/subtraction (DAA, DAS) Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfer between the accumulator and system register, or data memory can be performed.

1.4. Stack

A group of registers are used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine call and interrupt requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, and the bottom of stack will be shifted out.

2. ROM

The SH6620A can be addressed up to 1024 X 16 bit of program area from $000 to $3FF.
Service routine as the starting vector address.

Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as the starting vector address.

Address	Instruction	Remarks
$000H	JMP instruction	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP instruction	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP instruction	Jump to PBC service routine

3. RAM

Built-in RAM consists of general-purpose data memory and a system register. Direct addressing in one instruction can access data memory and the system register.

The following is the memory allocation map:
$000 ~ $01F: System register and I/O.
$020 ~ $05F: Data memory (64 X 4 bits).

The configuration of the system register is as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Pre-scaler)
$03	-	-	-	-	-	Reserved.
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low digit
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	-	-	Reserved
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 ~ 0) 1010: LPD Enable (Default) 0101: LPD Disable
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B ~ $0D	-	-	-	-	-	Reserved.
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13 ~ $15	-	-	-	-	-	Reserved.
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port
$19 ~ $1B	-	-	-	-	-	Reserved.
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge, Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	WDT	-	-	-	W	Bit3: WDT time-out bit (write one only)
$1F	-	-	-	-	-	Reserved

* Please refer to SH6610C user's manual for the System Register $00 ~ $12

Low Power Detection (LPD)

The LPD function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by the software control.

- If high reliability is not required
- If power supply voltage is V_{DD} = 2.2 to 6.0 V
- If operating ambient temperature is T_A = -20℃ to + 70℃

Functions of LPD Circuit

The LPD circuit has the following functions:

- Generates an internal reset signal when $V_{DD} \leq V_{LPD}$.
- Cancels the internal reset signal when $V_{DD} > V_{LPD}$.

Below, V_{DD}: power supply voltage, V_{LPD}: LPD detect voltage, it is about 1.6 ~ 1.7V and lower than V_{DD}-MIN (2.2V).

LPD Control Register

The LPD circuit is controlled by software enable flag.

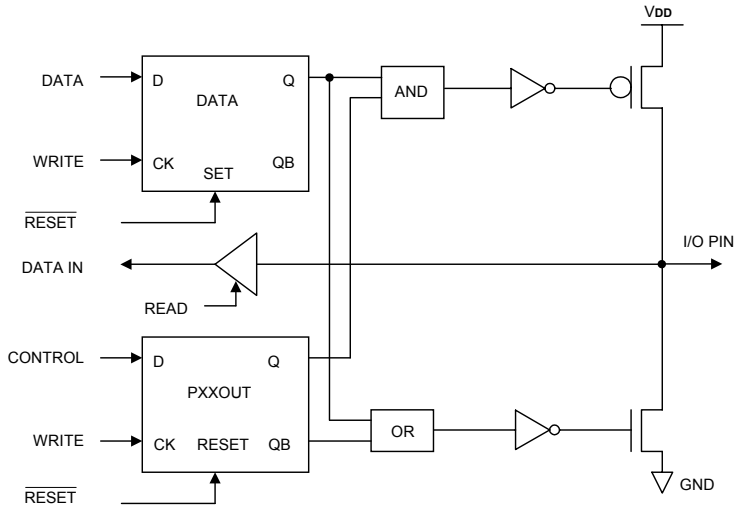
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$07	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 ~ 0): 1010: LPD Enable (Default); 0101: LPD Disable

LPD3、	LPD2、	LPD1、	LPD0：	LPD Enable/Disable flag．
1	0	1	0	Enable LPD circuit (Power-on initial)．
0	1	0	1	Disable LPD circuit．

System register $16 - $18

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port

Equivalent circuit for a single I/O pin



I/O control register:
PAXOUT, PBXOUT, PCXOUT (X = 0, 1, 2, 3)
1: Set I/O as an output buffer.
0: Set I/O as an input buffer (Power on initial).

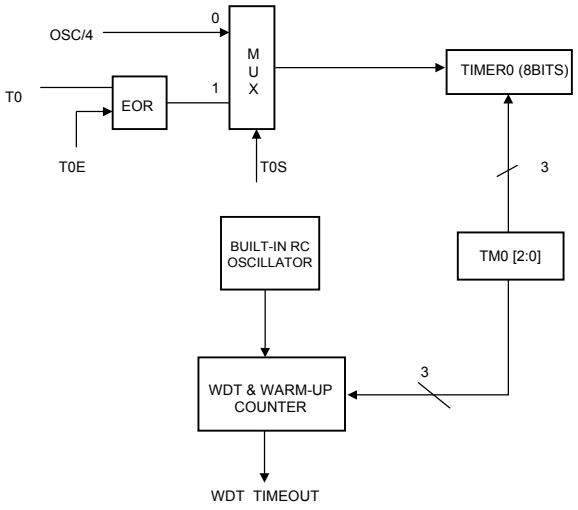
T0 & WDT

System Register $1C

Address	BIT3	BIT2	BIT1	BIT0	R/W	Remarks
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge. Bit1: T0 signal source.

T0E: T0 signal edge.
0: Increment on low-to-high transition T0 pin (Power on initial).
1: Increment on high-to-low transition T0 pin.

T0S: T0 signal source.
0: OSC 1/4 (Power on initial).
1: Transition on T0 pin.



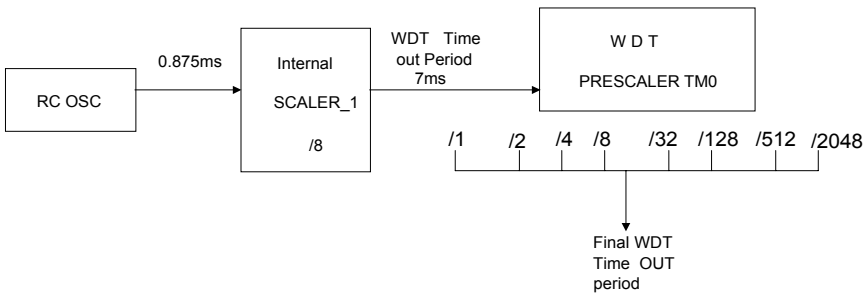
System register $1E

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1E	WDT	-	-	-	W	Bit3: WDT time-out bit (write one only)

The input clock of watchdog timer is generated by a built-in RC oscillator. Thus, the WDT will always run even in the STOP mode. SH6620A generates a RESET condition when the watchdog times-out. The watchdog can be enabled or disabled permanently by user option. To prevent it timing out and generating a device RESET condition, you can write this bit as "1" before timing-out. The WDT has a time-out period of more than 7ms (V_{DD} = 5V). If longer time-out periods are needed, a per-scaler with a division ratio of up to 1:2048 can be assigned to the WDT under the software control by writing to the TM0 register.

Pre-scaler divide ratio (valid for V_{DD} = 5V):

TM0.2	TM0.1	TM0.0	Pre-scaler divide ratio	Timer-out period
1	1	1	1:1	7ms
1	1	0	1:2	14ms
1	0	1	1:4	28ms
1	0	0	1:8	56ms
0	1	1	1:32	224ms
0	1	0	1:128	896ms
0	0	1	1:512	3,584ms
0	0	0	1:2048 (Power on initial)	14,336ms

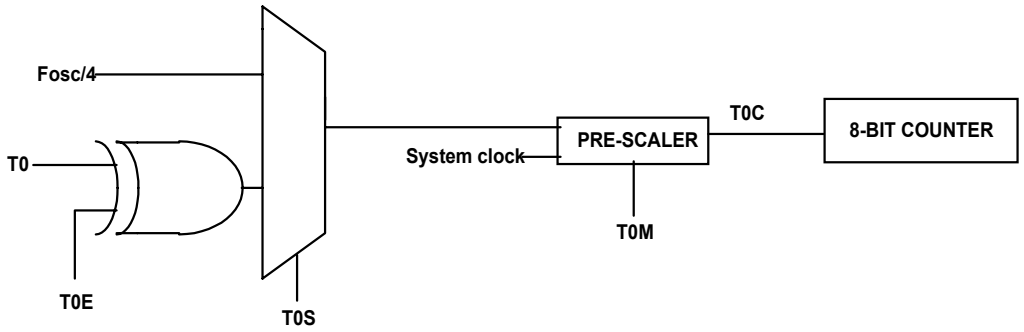


4. Timer0

SH6620A has one 8-bit timer. The timer/counter has the following features:

8-bit timer/counter
Readable and writable
Automatic re-loadable counter
8-prescaller scale is available
Internal and external clock select
Interrupt on overflow from $FF to $00
Edge select for external event

Following is a simplified timer block diagram:



4.1. **Configuration and Operation**

Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have LOW order digits and HIGH order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H). Load register programming: Write the LOW order digit first and then the HIGH order digit. The timer counter is loaded with the contents of load register automatically when the HIGH order digit is written or counter counts overflow from $FF to $00.

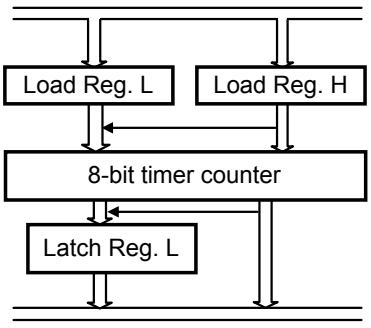
Timer Load Register: Since register H controls the physical READ and WRITE operation, please follow these rules:

Write Operation:

Low nibble first;
HIGH nibble to update the counter.

Read Operation:

High nibble first;
LOW nibble following.



4.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to wake the CPU from HALT mode.

4.3. Timer0 mode register

The timer can be programmed in several different pre-scaler ratios by setting the Timer Mode Register (TM0). The 8-bit counter counts pre-scaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in Table1. These mode registers select the input pulse sources into the timer.

Table 1: Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Pre-scaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{4}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

4.4. External Clock/Event T0 as TMR0 Source

When an external clock/event input is used for TM0, it is synchronized with the CPU system clock. Therefore, the external source must follow certain constrains. The output from T0M multiplex is T0C. It is sampled by the system clock in instruction frame cycle. Thus, it is necessary for T0C to be HIGH for at least 2 t**osc** and LOW for at least 2 t**osc**. When the pre-scaler ratio selects /20, T0C is the same as the system clock input. The requirement is as follows:

T0H = T0CH = T0 high time $\geq$ 2 t**osc** + ΔT

T0L = T0CL = T0 low time $\geq$ 2 t**osc** + ΔT

When other pre-scaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and the pre-scaler output is symmetrical.

Then:

$$\text{T0C high time} = \text{T0C low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = pre-scaler value

The requirement is, therefore:

$$\frac{N * T0}{2} \geq 2\ t\mathbf{osc} + \Delta T \text{ , or } T0 \geq \frac{4 * tosc + 2\Delta T}{N}$$

The limitation is applied for T**0** period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0 = Timer0 period} \geq \frac{4 * tosc + 2\Delta T}{N}$$

5. Port Interrupt

PBC interrupt (PORTB & C 8bits, falling edge) is controlled by Port I/O register. Only Input Port has Port Interrupt. Thus, if an interrupt enable flag IEP is set to 1 & one port bit high goes low been touched and that the condition is the other port bits are high level.

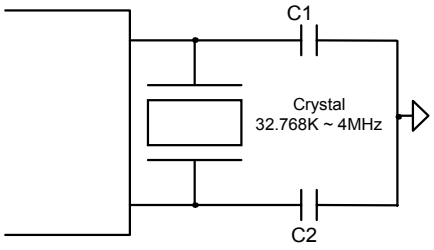
6. System Clock and Oscillator

System clock generator produces the basic clock pulses that provide the system clock with CPU and peripherals.

Instruction cycle time
(1) 4/32.768KHz (≈ 122us) for 32.768KHz system clock.
(2) 4/4MHz (= 1us) for 4MHz system clock.

Oscillator

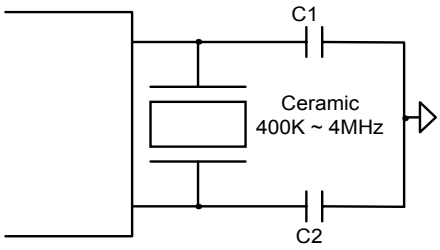
(1) Crystal oscillator: 32.768KHz - 4MHz.



C1, C2 Setting :

Crystal 32.768KHz :
C1, C2 < 56p (V_{DD} = 5V);
C1, C2 < 56p (V_{DD} = 3V).
Crystal 4MHz :
C1, C2 < 33p (V_{DD} = 5V);
C1, C2 < 10p (V_{DD} = 3V).

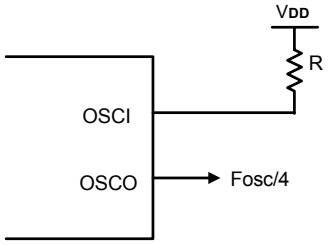
(2) Ceramic resonator: 400KHz - 4MHz.



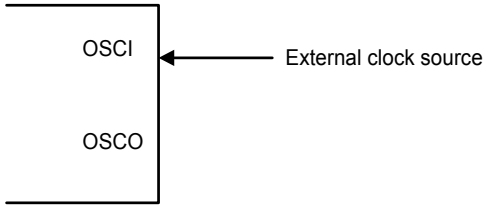
C1, C2 Setting :

Ceramic 400KHz :
20p < C1, C2 < 470p (V_{DD} = 5V);
20p < C1, C2 < 150p (V_{DD} = 3V).
Ceramic 4MHz :
20p < C1, C2 < 100p (V_{DD} = 5V);
C1, C2 < 10p (V_{DD} = 3V).

(3) RC oscillator: 400KHz - 4MHz.



(4) External input clock: 30KHz - 4MHz.



LPD (Initial States)

Hardware	After power-on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
System register	Undefined
AC	Undefined
Timer counter	0
Timer load register	0
WDT counter	0
WDT pre-scaler	0
I/O ports	Input
T0S T0E	00
WDT	0
LPD	1010

Instruction Set

All instructions are one cycle and one word instructions. The characteristic is memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] →CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. The same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not including p)	
RTNW H; L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Option (By ROM code)

Code Option

1. OSC:

osc2	osc1	osc0	OSC type
0	0	0	External (Default)
1	0	0	RC
1	1	0	X'tal 400K ~ 4MHz
1	0	1	Ceramic
1	1	1	X'tal 32.768KHz

2. WDT_EN:

0: Enable (Default)；

1: Disable．

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to + 7.0V

Input/Output Voltage . . . . . .GND -0.2V to V_{DD} + 0.2V

Operating Ambient Temperature . . . . . -10℃ to + 60℃

Storage Temperature . . . . . -55℃ to + 125℃

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	4.5		6	V	
Operating current	I_{OP}		1	2	mA	All output pins unloaded (Execute NOP instruction).
Stand by current (HALT)	I_{SB1}			0.5	mA	All output pins unloaded.
Stand by current (STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X} = I_{SB2} + 3uA). WDT off (If WDT on, I_{SB2X} = I_{SB2} + 15uA).
Input Low voltage	V_{IL1}	GND		0.2 X V_{DD}	V	I/O ports, pins tri-state.
Input Low voltage	V_{IL2}	GND		0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0.
Input Low voltage	V_{IL3}	GND		0.15 X V_{DD}	V	OSCI (Driven by external clock).
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD}	V	I/O ports, pins tri-state.
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$, T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}		V_{DD}	V	OSCI (Driven by external Clock).
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5	1	5	μA	GND < $V_{\overline{\text{RESET}}}$ < V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{t0} < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD} - 0.7			V	I/O ports, I_{OH} = -10mA, V_{DD} = 6.0V OSCO$_{RC}$, I_{OH} = -0.7mA, V_{DD} = 6.0V
Output Low Voltage	V_{OL}.			GND + 0.6	V	I/O ports, I_{OL} = 20mA, V_{DD} = 6.0V OSCO$_{RC}$, I_{OL} = 1.6mA, V_{DD} = 6.0V

AC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC1}			1	s	X'tal Osc = 32.768KHz, V_{DD} = 5.0V (for refer.)
Oscillator start time	T_{OSC2}			20	ms	Ceramic Osc = 400KHz, V_{DD} = 5.0V (for refer)
Oscillator start time	T_{OSC3}			2	ms	RC Osc = 400KHz, V_{DD} = 5.0V (for refer)
WDT period	T_{WDT}	7			ms	V_{DD} = 5.0V
Frequency stability (crystal)	Δ F/F			1	PPM	Crystal oscillator: [F(5.0) - F(4.5)]/F(5.0)
Frequency variation (crystal)	Δ F/F			10	PPM	Crystal oscillator: C1 = C2 = 5 ~ 30P
Frequency stability (ceramic)	Δ F/F			0.1	%	Ceramic resonator Osc: [F(5.0) - F(4.5)]/F(5.0)
Frequency Variation (RC)	Δ F/F			± 20	%	Include supply voltage and chip to chip variation

User Notice: Max. Current into V_{DD} = 50mA;
Max. Current out of V_{SS} = 150mA
Max. Output current sunk by any I/O port = 25mA;
Max. Output current sourced by any I/O port = 20mA
Max. Output current sunk by all ports (A, B, C) = 50mA;
Max. Output current sourced by all ports (A, B, C) = 40mA

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Operating voltage	V_{DD}	2.2		4.5	V	
Operating current	I_{OP}		0.7	1.3	mA	All output pins unloaded (Execute NOP instruction).
Stand by current (HALT)	I_{SB1}			0.2	mA	All output pins unloaded.
Stand by current (STOP)	I_{SB2}		1	2	μA	All output pins unloaded, LPD off (If LPD on, I_{SB2X} = I_{SB2} + 3uA). WDT off (If WDT on, I_{SB2X} = I_{SB2} + 5uA).
Input Low Voltage	V_{IL1}	GND		0.2 X V_{DD}	V	I/O ports, pins tri-state.
Input Low Voltage	V_{IL2}	GND		0.15 X V_{DD}	V	$\overline{\text{RESET}}$, T0.
Input Low Voltage	V_{IL3}	GND		0.15 X V_{DD}	V	OSCI (Driven by external clock).
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD}	V	I/O ports, pins tri-state.
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$,T0
Input High Voltage	V_{IH3}	0.85 X V_{DD}		V_{DD}	V	OSCI (Driven by external Clock).
Input Leakage Current	I_{IL1}	-1		1	μA	I/O ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5			μA	GND < $V_{\overline{\text{RESET}}}$ < V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	GND < V_{T0} < V_{DD}
Input Leakage Current	I_{IL5}	-3	1	3	μA	For OSCI
Output High Voltage	V_{OH}	V_{DD} - 0.7			V	I/O ports, I_{OH} = -7mA, V_{DD} = 3V OSC_{RC}, I_{OH} = -0.7mA, V_{DD} = 3V
Output Low Voltage	V_{OL}.			GND + 0.4	V	I/O ports, I_{OL} = 8mA, V_{DD} = 3V OSC_{RC}, I_{OL} = 1.0mA, V_{DD} = 3V

AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, F_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Oscillator start time	T_{OSC1}			1	s	Crystal Osc = 32.768KHz, V_{DD} = 3.0V.
Oscillator start time	T_{OSC2}			35	ms	Ceramic Osc = 400KHz, V_{DD} = 3.0V.
Oscillator start time	T_{OSC3}			5	ms	RC Osc = 400KHz, V_{DD} = 3.0V.
WDT period	T_{WDT}	7			ms	V_{DD} = 3.0V
Frequency stability (crystal)	Δ F/F			1	PPM	Crystal oscillator: [F(3.0)-F(2.7)]/F(3.0)
Frequency variation (crystal)	Δ F/F			10	PPM	Crystal oscillator: C1 = C2 = 5 ~ 30P
Frequency stability (ceramic)	Δ F/F			0.1	%	Ceramic resonator OSC:[F(3.0)-F(2.7)]/F(3.0)
Frequency Variation (RC)	Δ F/F			± 20	%	Include supply voltage and chip to chip variation

Operation frequency vs. I_{SB1}

I_{SB1X} = (Frequency /4MHz) × I_{SB1}

Operation frequency vs. I_{OP}

I_{OPX} = (Frequency /4MHz) × I_{OP}

32K Max. Halt current

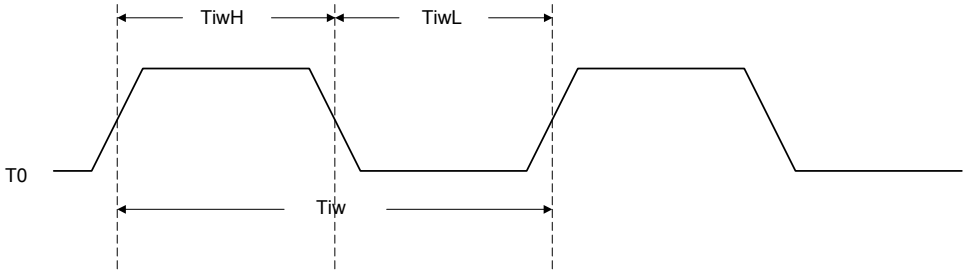
32KHz Halt current < 5uA@3V; (WDT is disabled)

AC Characteristics

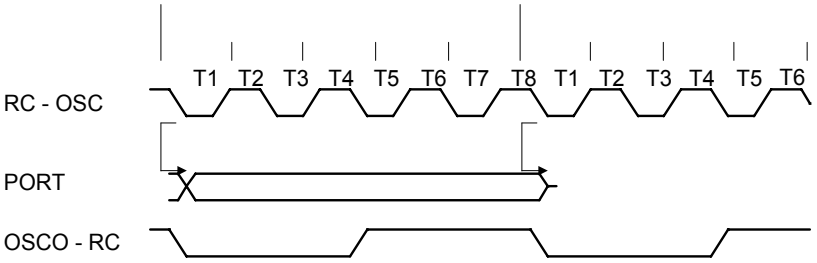
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CY}	Instruction cycle time	1		122	μs	
T_{IW}	T_0 input width	(T_{CY} + 40)/N			ns	N = Pre-scaler divide ratio.
T_{IWH}	High pulse width	1/2 t_{IW}			ns	
T_{IWL}	LOW pulse width	1/2 t_{IW}			ns	

Timing Waveform

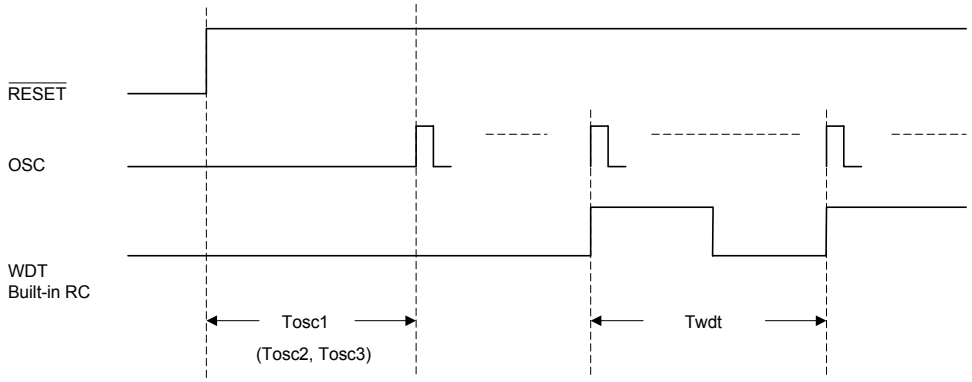
T_0 Input Waveform



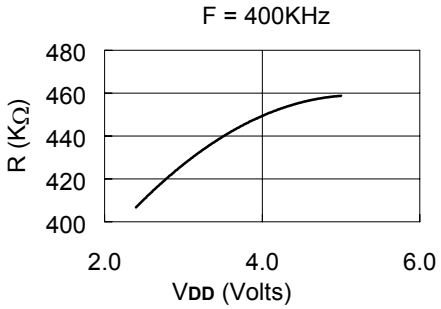
RC OSCO Timing Waveform

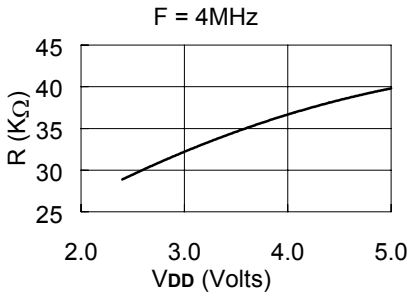


Built-in RC Oscillator

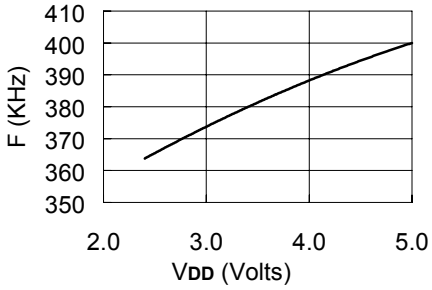


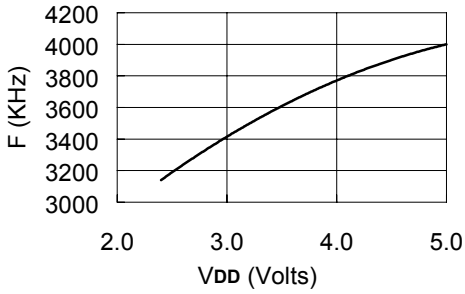
Typical RC oscillator Resistor vs. V_{DD}: (for reference only)



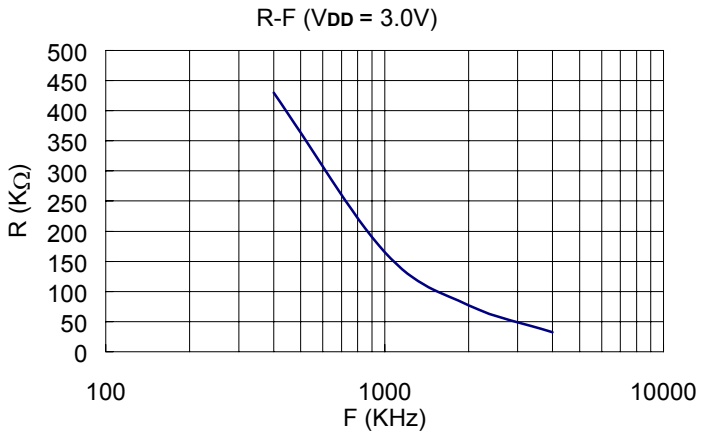


Typical RC oscillator Frequency vs. V_{DD}: (for reference only)





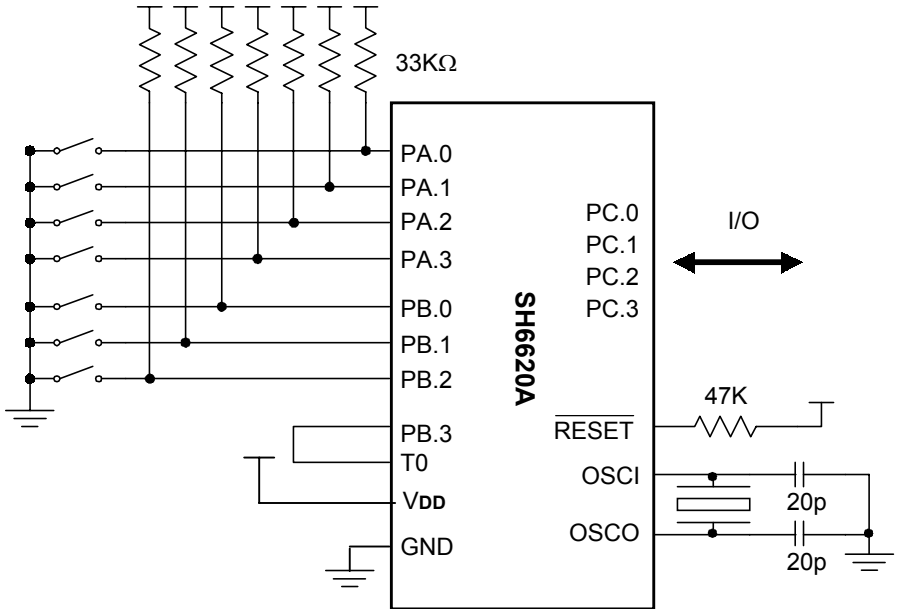
Typical RC oscillator Resistor vs. Frequency: (for reference only)



Application Circuits (for reference only)

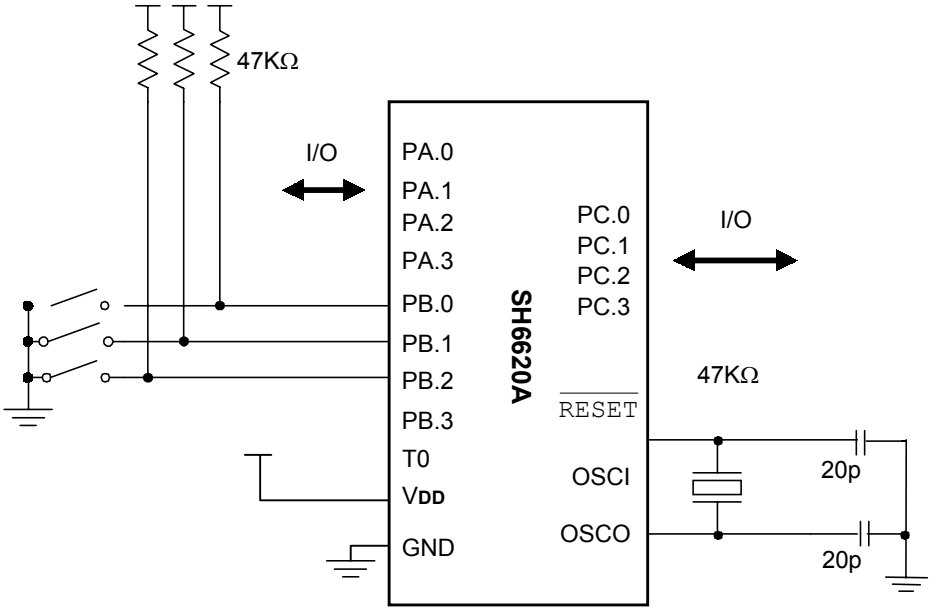
AP1:

a. Operating voltage: 3.0V.
b. Oscillator: Crystal 32.768KHz.
c. PORTA - C: I/O.



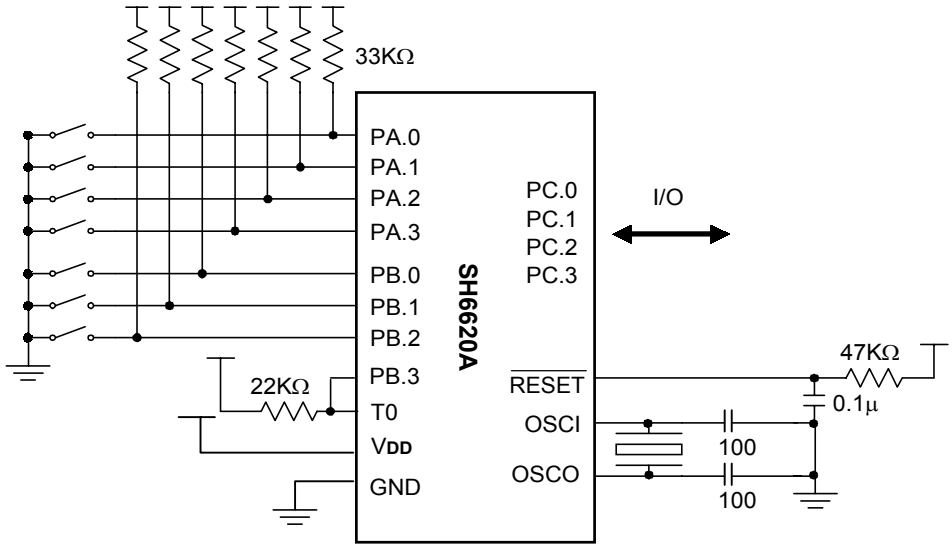
AP2:

a. Operating voltage: 5.0V.
b. Oscillator: Crystal 4MHz.
c. PORTA - C: I/O.



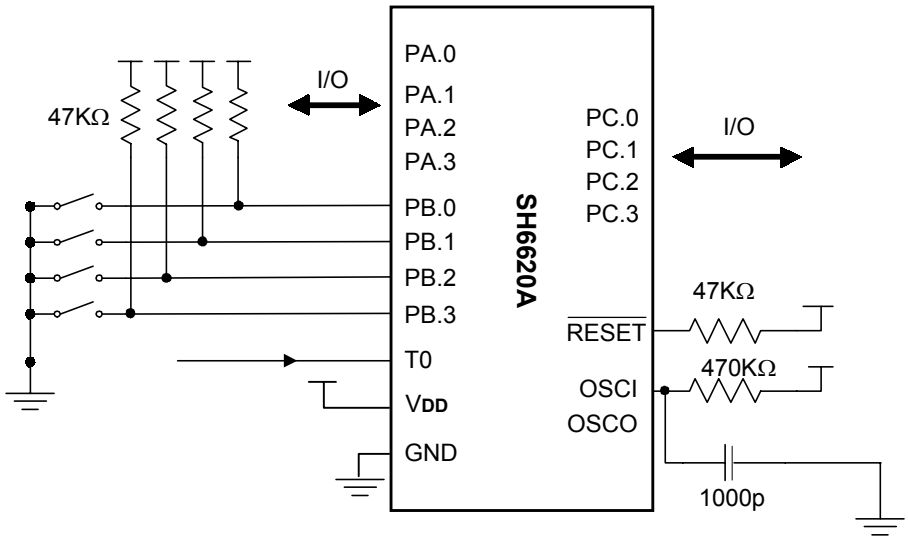
AP3:

a. Operating voltage: 5.0V.
b. Oscillator: Ceramic 400KHz.
c. PORTA - C: I/O.



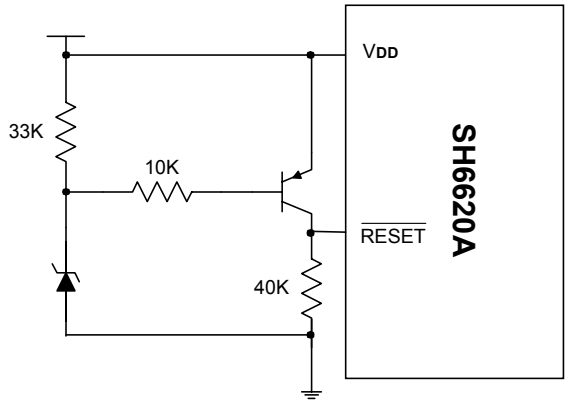
AP4:

a. Operating voltage: 5.0V.
b. Oscillator: RC 400KHz.
c. PORTA - C: I/O.
d. Timer0 input: T0.



AP5:

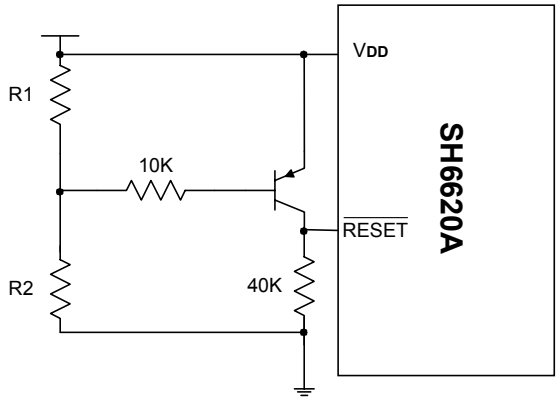
Reset Protection Circuit 1



$\overline{\text{RESET}}$ will be pulled to GND when V_{DD} goes lower than Zener voltage + 0.7V.

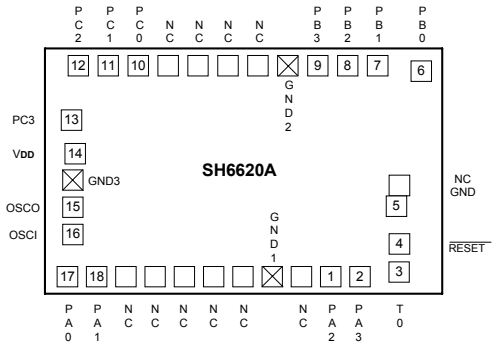
AP6:

Reset Protection Circuit 2



$\overline{\text{RESET}}$ will be pulled to GND when (V_{DD} X R1/(R1 + R2)) is lower than 0.7V

Bonding Diagram



NOTE:

1. GND1, GND2&GND3 BONDING TO GROUND.
2. SUBSTRATE CONNECT TO GROUND.

unit: μm

Pad No	Designation	X	Y	Pad No	Designation	X	Y
	GND1	164.40	-586.55	10	PC 0	-430.40	586.55
1	PA 2	422.80	-586.55	11	PC 1	-562.80	586.55
2	PA 3	543.80	-586.55	12	PC 2	-701.95	586.55
3	T0	700.60	-584.30	13	PC 3	-717.50	276.80
4	$\overline{\text{RESET}}$	700.60	-441.40	14	V_{DD}	-713.70	95.10
5	GND	697.80	-284.70		GND3	-717.05	-34.40
6	PB 0	754.40	537.75	15	OSCO	-717.05	-188.10
7	PB 1	605.50	586.55	16	OSCI	-717.05	-311.10
8	PB 2	485.50	586.55	17	PA 0	-721.30	-586.55
9	PB 3	353.10	586.55	18	PA 1	-598.80	-586.55
	GND2	213.75	586.55				

Ordering Information

Part No.	Package	Packing
SH6620AH-yyxxx/000HR	Chip Form	Tray
SH6620A-yyxxx/018DU	18L DIP	Tube
SH6620AM-yyxxx/018MU	18L SOP	Tube

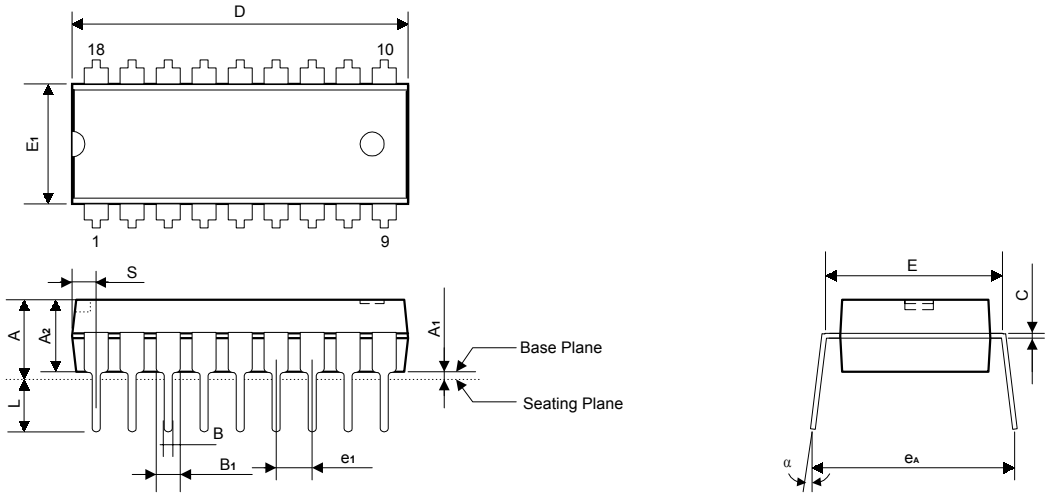
Note:

(1) "-yyxxx": "yy" means 2 bits option and "xxx" means 3 bits code seriary number. If the product is OTP type and in blank order, those bits should be none.
(2) The data after mark "/" in Part No. block is the package and packing information for ordering.
(3) The size of those package types are showed in "Package Information" (Page25 - Page26).
(4) Any other package or packing request, please refer to following table.

Package		Packing	
D	DIP	**R**	Normal package size and in tray packing
F	QFP	**U**	Normal package size and in tube packing
H	CHIP	**A**	Normal package size and in tape & reel packing
J	CER-DIP	**D**	Larger package size and in tray packing
K	SKINNY	**L**	Larger package size and in tube packing
L	PLCC	**B**	Larger package size and in tape & reel packing
M	SOP	**T**	Smaller package size and in tray packing
N	OTHER	**S**	Smaller package size and in tube packing
Q	GOOD DIE ON WAFER	**N**	Smaller package size and in tape & reel packing
S	SOJ		
T	TO92		
V	VSOP/TSOP		
W	WAFER		
X	TSSOP		

Package Information

DIP 18L Outline Dimensions unit: inches/mm

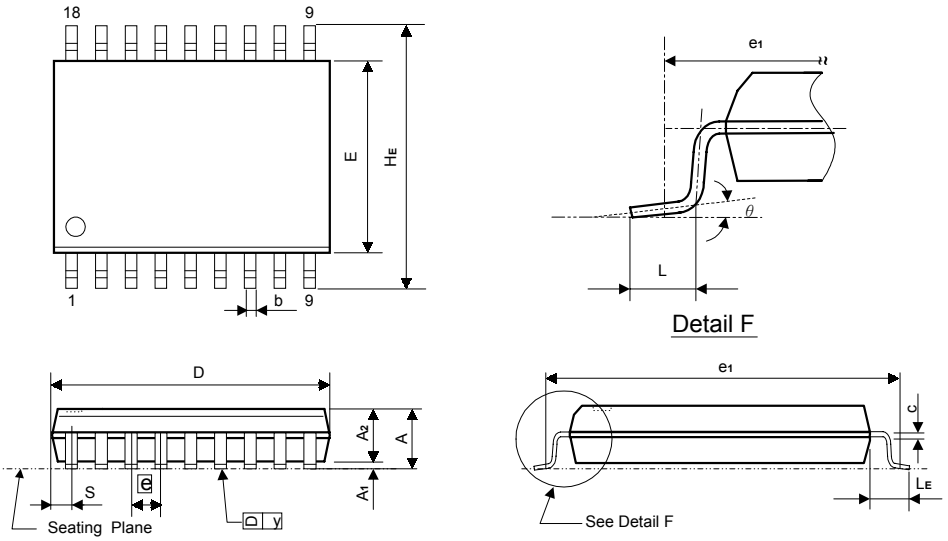


Symbol	Dimensions in inches	Dimension in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.900 Typ. (0.920 Max.)	22.86 Typ. (23.37 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.055 Max.	1.40 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 18L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.455 ± 0.015	11.56 ± 0.38
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.030 ± 0.008	0.76 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.037 Max.	0.94 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.5	Add package and packing information in ordering information	Jul. 2004
2.4	Change RC Frequency Variation to ±20%	Apr. 2002
2.3	Add Reset Protection Circuit (AP5 and AP6)	Feb. 2002
1.0	Original	Jul. 1999